Appln No. 09/637,846
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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A method of assigning ownership of a peripheral component interconnect (PCI) bus, the method including:

assigning a master a MEDIUM priority level, wherein the master is inactive until the master asserts a request signal when the master wants to take control of the PCI bus;

identifying a target requested by the master;

issuing a provisional grant to the master in response to the request signal;

determining if data associated with the target is available; and

assigning a first priority level for ownership of the PCI bus to the master if the data is not available and assigning a second priority level for ownership of the PCI bus to the master if the data is available.

2. (Canceled)

3. (Previously presented) The method of Claim 1, wherein assigning a first priority level for ownership of the PCI bus to the master if the data is not available comprises

assigning a LOW priority level to the master if the data is not available.

4. (Previously presented) The method of Claim 1, wherein assigning a second priority level for ownership of the PCI bus to the master if the data is available comprises assigning a HIGH priority level to the master if the data is available.

5. (Original) The method of Claim 1, wherein the target uses delayed transactions to complete a read access.

6. (Original) The method of Claim 5, wherein the target integrates a buffer management scheme.

7. (Original) The method of Claim 6, wherein the buffer management scheme includes an input/output cache.

8. (Previously presented) The method of Claim 1, wherein identifying a target includes sending the request signal from the master to an arbiter.

9. (Previously presented) The method of Claim 8, wherein assigning a second priority level includes sending a modified request signal to the arbiter.

10. (Currently amended) A method of assigning priority to a master on a peripheral component interconnect (PCI) bus, comprising:

assigning a MEDIUM priority to the master;

posting a request by the master to an arbiter to take control of the PCI bus;

issuing a provisional grant by the arbiter to the master;

determining whether data is available from a target associated with the request;

if the data is not available, assigning a LOW priority to the master, wherein the LOW priority is maintained until the data becomes available; and

if the data is available, assigning a HIGH priority to the master;

wherein the master is inactive between assigning a MEDIUM priority and posting a request.

11. (Canceled)

12. (Previously presented) The method of claim 10, further comprising modifying the request if the data is available, and sending the modified request to the arbiter.

13. (Previously presented) The method of claim 12, further comprising if the PCI bus is available, and no other HIGH priority masters have earlier rights to the PCI bus,

issuing a final grant by the arbiter to the master to allow the master to take control of the PCI bus.

14. (Previously presented) The method of claim 13, further comprising changing the priority of the master back to the MEDIUM priority after transferring the data from the target.

15. (Currently amended) A peripheral component interconnect (PCI) bus system comprising:

a PCI bus;

a plurality of masters coupled to the PCI bus, each said master being initially assigned a MEDIUM priority;

a plurality of targets coupled to the PCI bus; and

an arbiter which assigns ownership of the PCI bus to said masters,

wherein the arbiter issues a preliminary grant to one said master, which posts a request to control the PCI bus to access one said target,

wherein if data is not available from the one said target, the arbiter assigns a LOW priority to the one said master, wherein the LOW priority is maintained until the data becomes available, [[and]]

wherein if the data is available from the one said target, the arbiter assigns a HIGH priority to the one said master,

<u>wherein the one said master is inactive after being assigned the MEDIUM priority until the one said master posts the request to control the PCI bus</u>.

16. (Canceled)

17. (Currently amended) The [[method]] peripheral component interconnect (PCI) bus system of claim 15, wherein the one said master modifies the request if the data is available, and sends the modified request to the arbiter.

18. (Currently amended) The [[method]] peripheral component interconnect (PCI) bus system of claim 17, wherein if the PCI bus is available, and no other HIGH priority masters have earlier rights to the PCI bus, the arbiter issues a final grant to the one said master to allow the one said master to take control of the PCI bus.

19. (Currently amended) The [[method]] peripheral component interconnect (PCI) bus system of claim 18, wherein the arbiter changes the priority of the master back to the MEDIUM priority after the data has been transferred from the target.